

Ingenic®

T41 Hardware Design Checklist

Date: Jun.2022

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Release history

Date	Revision	Change
Jun.2022	1.0	First release

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1 Checklist

1.1 Design Requirements on the Clock Circuit of the Master Chip

Number	Items	Customer Confirmation (YES/NO)	Notes
1	The master chip needs to connect to a 24 MHz external clock with the maximum deviation of ± 30 ppm.		
2	The external passive crystal is connected, the starting resistor of 1M and the 33R current limiting resistor cannot be omitted .		
3	It is recommended to choose 4-pin encapsulated passive crystal, of which 2 pins are grounded(GND) to enhance the anti-interference ability of ESD.		
4	The traces of the crystal signals (Xin, Xout) are as short as possible and are surrounded with ground (GND) traces, The reference plane must be kept intact, The high-speed signal traces cannot be routed under the crystal circuit, Have as many ground vias around the crystal as possible.		

1.2 Design Requirements on the Reset Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 supports internal POR reset and external hardware reset of PPRST_ pin. The reset mode is determined by the level of POR_CTL pin. POR_CTL pin is high, internal POR reset, POR_CTL pin is low, external hardware reset.		
2	When the POR_CTL pin is pulled up, it needs to be pulled to 1.8V through the external resistor. Select the internal POR reset and the PPRST_ pin is suspended.		
3	When the POR_CTL pin is pulled low, it can be directly connected to GND and select external hardware reset through PPRST_ pin. RC reset circuit is recommended for hardware reset. The power supply of R resistor is 1.8V, and the shorter the wire of PPRST_ pin, the better.		
4	RST_OUT is not recommended to connect to the RST PIN of Flash, because the RST_OUT signal level is 1.8V, and the RST PIN of Flash is 3.3V, so the RST_OUT signal can be suspended.		

1.3 Design Requirements on the BOOT Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	There are 4 ways to start T41 BOOT. The configuration method is determined by BOOTSEL0 and BOOTSEL1 level. The power domain of the two pins belongs to 3.3V.		

2	BOOT configuration mode: BOOTSEL1, BOOTSEL0 00: SD BOOT 01: Flash BOOT (default) 10: Uart BOOT 11: USB BOOT		
3	If the two Bootsel pins need to be operated frequently production testing, it is recommended to connect a 1K resistor on the two pins to increase the ability of anti-ESD.		

1.4 Design Requirements on the DDR Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 built-in DDR3 particles, the DDR part of the main consideration of power supply design.		
2	DDR ZQ resistor should be connected with 240R 1% resistor and placed close to the pin.		
3	The DDRVREF voltage is derived from the DDRVDD voltage partial voltage through two resistors with the same accuracy of 1%. The voltage value is $\frac{1}{2}$ of the DDRVDD voltage, and the recommended resistance is 100K/1%.		
4	The DDRMEM and DDRVDD voltages are selected according to the type of built-in DDR particles. The DDR3 voltage is 1.5V and the DDR3L voltage is 1.35V.		
5	DDRPLL_VCCA is a DRR PLL power supply with a typical voltage of 1.8V. It is recommended to isolate it from the system with a magnetic bead of 1.8V.		

1.5 Design Requirements on the FLASH Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	When T41 starts FLASH through SFC interface, NOR FLASH or NAND FLASH can be selected. If you need to start FLASH quickly, it is recommended to choose NOR FLASH.		
2	SFC interface can be started by either single wire or four wire. If you need quick start, it is recommended to choose four wire start.		
3	SFC_CLK recommends that the source endpoint be connected in series with 33R resistors, adjust the signal impedance and reserve EMI debugging problems, and the routing should be surrounded with ground(GND) in the whole process.		
4	The shorter the wiring of the 6 wires of the SFC interface, the better, and the adjacent reference layer should be kept intact. If the wiring is too long (over 600MIL), it is suggested to do equal length treatment.		

1.6 Design Requirements on the DEBUG Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	By default, UART1 is used for serial port debug of T41, and the power domain is 3.3V. During design, the level of external equipment should be matched.		
2	The default UART1 serial port debug is not recommended to be modified to other UART ports, If modified, the		

	corresponding firmware also needs to be modified, which is not conducive to firmware management.		
3	When UART1 is debugged as a serial port, reuse of UART1 functions on other pins is not recommended .		
4	UART1 RX signal needs to be connected with 10K resistor to 3.3V to prevent the serial port from printing garble code. For RX TX signal, 33R resistors in each series are recommended at the DEBUG connector to enhance the anti-ESD ability of the signal.		

1.7 Design Requirements on the RTC circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	A 32.768KHz oscillator is built in T41. When using RTC function, an external 32.768k crystal and matching capacitor are required.		
2	When RTC clock uses active crystal, from pin OSC32_ XI input, pin OSC32_ OUT suspension processing.		
3	VDD_ RTC uses 0.8V for power supply. When using button battery for power supply, LDO with low quiescent current should be used to reduce voltage to VDD_ RTC use.		
4	VDDIO_ RTC uses 1.8V for power supply. When using button battery for power supply, LDO with low quiescent current should be used to reduce voltage to VDDIO_ RTC use.		

1.8 Design Requirements on the I2C Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	I2C signal SCL and SDA are OD output pins, which need to be connected with pull-up resistors. The pull-up resistors should be selected according to different bus loads and PCB layers. It is recommended to choose a pull-up resistance of 1K to 10K.		
2	The I2C interfaces reused by T41 include SMB0, SMB1, SMB2 and SMB3, and the PIN power domain reused by each I2C interface is also different. Attention should be paid to the level matching when using.		
3	After each I2C interface is used, reuse of the same set of I2C functions on other PINs is not recommended.		

1.9 Design Requirements on the DVP/BT video input circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 supports a single-channel DVP SENSOR interface. The interface level of the SENSOR is configured to support 1.8V, which is configured by the VDDIO3318_2 power pin. The interface level should match the IO level of the external SENSOR.		
2	DVP interface supports 8bit, 10bit input, low alignment, to ensure that the signal connection is one-to-one correspondence.		
3	DVP SENSOR CLK is input by SA1_DVP_MCLK_PA15, I2C communication port is input by		

	I2C0 (SD6_SMB0_SDA_PA12, SD7_SMB0_SCK_PA13) control, I2C0 signal needs to be connected to the pull resistor.		
4	T41 supports single channel BT signal input, BT1120 and BT656, BT1120 only supports 8bit serial mode, input pin and DVP signal input pin multiplexing, so the two can only choose one way as input.		
5	BT1120 signal input by DVP_D0--DVP_D7 access, BT656 signal input by DVP_D0--DVP_D7 access, ensure that the signal connection is one-to-one correspondence, the signal level and the external device level match.		
6	DVP and BT signals are recommended to be routed in the same layer. If the routed signal is too long, equilength processing is recommended.		

1.10 Design Requirements on the MIPI CSI video input circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 supports single-channel 4Lane or single-channel 2Lane MIPI signal SENSOR interface input, and the interface voltage only supports 1.8V.		
2	The single-channel 4Lane MIPI signal is connected by CLK0 and DATA0--DATA3 differential signals, and the DATA1 differential clock is suspended.		
3	Single channel of 2Lane MIPI access. A route is CLK0, DATA0--DATA1 differential signal access.		

4	When the single-channel 1 Lane or 2 lane MIPI SENSOR is input, the SENSOR CLK is input by SA1_DVP_MCLK_PA15, the I2C communication port is controlled by I2C0(SD6_SMB0_SDA_PA12, SD7_SMB0_SCK_PA13), and the I2C1 signal needs to be connected with a pull up resistor.		
5	During the routing of MIPI signals, the adjacent reference layer should be kept intact and not cross two planes. The routing of signals between adjacent groups should be surrounded with ground (GND) traces, and it is better to use GND via for isolation.		
6	The differential impedance of MIPI signal was controlled at 100Ω, the trace length deviation within the differential signal group was controlled within ±5mil, and the trace length deviation between the groups was controlled within ±100mil (the line length of the clock signal was used as the reference)		

1.11 Design Requirements on the SD CARD Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	By default, T40 uses MSC0 interface as SD CARD communication interface, and the MSC0 interface voltage only supports 3.3V.		
2	It is suggested that the SD Card power supply should use MOSFET to control the power up and down. The low level is effective, and a separate CARD power up and down PIN is needed to control it.		

3	CMD, D0-- D3 of MSC0 interface need to connect pull up resistors to the card power supply, the recommended resistance is 10K- 100K.		
4	When using the SD CARD function, the SD_CARD_DETECT signal must be connected to the SD CARD DETECT pin, reserving 100K Ω to pull up resistor to 3.3V of the system power, and cannot be suspended.		
5	In multi-layer board design, the routing reference plane of MSC0_CLK, DATA and CMD signals should be kept intact. CLK routing should be surrounded with ground (GND) traces. If the routing is too long, equilelength processing is recommended.		
6	MSC0_DATA and CMD pull up resistors should be placed nearby to avoid excessively long stubs on wires, which may affect the signal quality.		
7	Considering that the instantaneous demand current of SD CARD is relatively large when it is working, the power line should be maintained above 30mil, and the MOSFET control power supply should have a slow start. 100NF capacitor can be parallel connected between the gate and source of the MOSFET.		

1.12 Design Requirements on the MSC1 Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 multiplexed MSC1 signal on two GPIO groups, PB17-- PB22 and PC02-- PC17. MSC1 signal in PB group only supported 3.3V, and MSC1 signal in		

	PC group only supported 1.8V/3.3V.		
2	The MSC1 signal of PB group has no anti-leakage function, while the MSC1 signal of PC group has anti-leakage function. Therefore, the MSC1 signal of PC group can be given priority when making low-power scheme.		
3	MSC1 signal can be connected to WiFi module and EMMC module. When the external device is connected, the group of MSC1 signals should be selected according to the IO level of the device.		
4	MSC1 signals of PB group and PC group belong to the same SDIO controller, and they cannot be used at the same time.		
5	CMD, D0-- D3 of MSC1 interface need to connect pull up resistors to the card power supply, the recommended resistance is 10K- 100K.		
6	In multi-layer board design, the routing reference plane of MSC1_CLK, DATA and CMD signals should be kept intact. CLK routing should be surrounded with ground (GND) traces. If the routing is too long, equilength processing is recommended.		
7	MSC1_DATA and CMD pull up resistors should be placed nearby to avoid excessively long stubs on wires, which may affect the signal quality.		

1.13 Design Requirements on the SPI Master Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 multiplexed SPI0 signals on two GPIO groups, P06---PA11 and PC02---PC07. PA group only supported 1.8V, PC group supported 1.8V/3.3V.		
2	SPI0 signals of PA group have no anti-leakage function, while SPI1 signals of PC group have anti-leakage function. Therefore, SPI1 signals of PC group can be given priority when making low-power solution.		
3	SPI0 signal can be connected to the WIFI module or the device with SPI communication interface. When connecting the external device, the set of SPI1 signals should be selected according to the IO level of the device.		
4	SPI0 signals of PA group and PC group belong to the same SPI controller, and they cannot be used at the same time.		
5	SPI1 signal multiplexing on PA20---PA22&PA29---PA31 and PB25---PB30 GPIO belongs to 3.3V power supply domain and does not have leakage protection function.		

1.14 Design Requirements on the SPI Slave Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 has a set of SPI slave on PC15---PC18 GPIO. SPI Slave signals in PC group support 1.8V/3.3V.		

2	SPI Slave signals of PC group have leakage prevention function. Therefore, SPI Slave signals of PC group can be given priority when making low-power solution.		
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1.15 Design Requirements on the UART Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 has five UART interfaces, UART and UART2 can support hardware flow control. Except for UART1 as DEBUG, the other four channels can be used as UART communication interfaces.		
2	UART reuse PIN can query T41 DS documents, and it needs to keep matching with peripheral IO port level during use.		
4	UART0 GPIO PC08---PC12, UART2 GPIO PC13, PC14, PC19, PC20 support 1.8V/3.3V,, with anti-leakage function, which can be preferred when making low power solution.		
5	Cross connection of RX and TX signals is required for UART signal connection. For example, the TX signal of the device needs to be connected to the RX of T41.		
6	Cross connection of RTS and CTS signals is required for the connection of UART hardware flow control signals. For example, the CTS signal of the device needs to be connected to the RTS of T41.		

1.16 Design Requirements on the DMIC Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 supports 4 channels of digital MIC input at the same time, which can be used for sound source positioning.		
2	PC28-- PC30 GPIO multiplexed DMIC signal only supports 3.3V, with leakage prevention function.		
3	GPIO PA14, PA16, PA17 multiplexed DMIC signal supports 1.8V, without leakage protection function.		
4	DMIC CLK signal routing requires 33R resistors in series at the source endpoint, and the signal needs to be surrounded with ground (GND) traces,		

1.17 Design Requirements on the Ethernet Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 has built-in 10/100Mbps Ethernet controller, it supports built-in voltage type phy and external PHY external circuits. There is and can only use one built-in PHY or external PHY circuit, and only supports RMII mode in communication mode.		
2	When using external PHY, PHY_CLK, TXD [0:1] signals suggest a 33R resistor in series at the source endpoint to adjust the impedance.		
3	PHY_CLK is the output signal that provides the master clock for PHY, TX_CLK is the input signal that sends the sampling clock, and external PHY needs to be configured		

	to the corresponding mode. For example, RTL8201 PHY REF_CLK needs to be configured to the output mode.		
4	The MDIO signal requires an external 10K resistor to the PHY 3.3V power supply, ensuring that the signal default level is high.		
5	PHY_CLK, TX_CLK signal is routed, It needs to be as short as possible and are surrounded with ground (GND) traces, and the adjacent reference layer shall be kept intact.		
6	RXDV and RXD[0:1] signals need to be routed at the same layer. If the routed signal is too long, equal length processing is needed (based on TX_CLK line length).		
7	TXEN, TXD[0:1] signals need to be routed at the same layer. If the routed is too long, equal length processing is needed (based on TX_CLK line length).		
8	When using the built-in PHY, PHY_RST needs to use GPIO alone to control PHY soft reset.		
9	RBIAS pin needs to be externally connected with a resistance of 2.49k (1% accuracy) to the ground.		
10	DVDD1V2OYT and AVDDL_REG suggests connecting 1uF and 0.1uF capacitor close to the pin respectively.		
11	RXD3, RX_DV, EN_LDO, pin hardware configuration can refer to the recommended hardware design.		
12	When using RMI network, GMAC_MDCK (pin R10) and GMAC_MDIO (pin T10) can only be used as MDIO interface, and GMAC_MDIO (pin T10) needs to be pulled up to 3.3V and cannot be used for other functions.		

1.18 Design Requirements on the SADC Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 built-in 12bit successive approximation ADC, can support 4 ADC channels input at the same time.		
2	The sampling range of 4-channel ADC voltage is 0--1.8V, and the sampling voltage shall be guaranteed within the normal range to ensure the accuracy of ADC sampling.		
3	When the photosensitive voltage is collected by ADC, it should be ensured that the photosensitive voltage is fast and stable to achieve real image display.		
4	When ADC input signal is routed, it shall be processed in the manner of analog signal. The shorter the routed, the better. Cannot walk line with digital signal, should be surrounded with ground (GND) traces, and the adjacent reference layer shall be kept intact.		

1.19 Design Requirements on the USB Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 supports USB2.0 OTG and can be configured USB0ID signal. Default USB0ID is low level and USB is configured in Host mode.		
2	The USB0ID signal power domain is 1.8V. When USB is configured in Device mode, the USB0ID signal needs to be pulled up to 1.8V through resistor.		

3	USB DP/DM signal routing shall be processed as a differential signal, the differential impedance shall be controlled at 90Ω , the routing length deviation within the differential signal group shall be controlled within $\pm 5\text{mil}$, and the adjacent reference layer shall be kept intact.		
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1.20 Design Requirements on the CODEC Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	The filter capacitor on the VCM pin is a combination of $100\text{nF} + 4.7\mu\text{F}$, and the two capacitors need to be placed close to the Master chip pin.		
2	The filter capacitor on the MICBIAS pin is a combination of $100\text{nF} + 4.7\mu\text{F}$, and the two capacitors need to be placed close to the Master chip pin.		
3	Separating capacitors should be placed on the MIC input signals of MICPL, MICNL. The value of separating capacitors is recommended to be 100nF and should be placed close to the Master chip pin.		
4	The 2.2K bias resistance of MIC shall be placed close to the MIC endpoint, and the filter capacitor of $4.7\mu\text{F}$ shall be placed close to the resistance endpoint.		
5	In order to obtain better audio quality, it is recommended to add audio amplifier and filter circuit to the periphery of audio output pin HPOUTL. For details, please refer to the hardware reference		

	schematic .		
6	In order to obtain a better audio MIC background noise, it is recommended to reserve a high PSRR LDO near the 2.2K bias resistor to provide the bias voltage directly.		
7	The wiring of MICPL, MICNL analog audio input signal, HPOUTL analog audio output signal, VCM signal, MICBIAS and other signals should be as short as possible. The wiring width is recommended to be 8-12mil, and it should be surrounded with ground (GND) traces. The adjacent reference layer should take GND layer as the reference and ensure the integrity of the reference layer, can't cross different planes.		

1.21 Design Requirements on the I2S Circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T40 multiplexed I2S signal on two groups of GPIO, PB08 -PB16 and PC11-- PC18. I2S signal in PB group only supports 3.3V and I2S signal in PC group supports 1.8V/3.3V. The signal level should be matching with the peripheral level.		
2	I2S signal of PB group has no anti-leakage function, while I2S signal of PC group has anti-leakage function. Therefore, I2S signal of PC group can be given priority when designing low-power solution.		
3	I2S signals of PB group and PC group belong to the same I2S controller, and they cannot be used at the same		

	time.		
4	MCLK signal needs 33R resistor in series at the source endpoint to adjust the impedance to obtain better signal quality.		
5	When I2S signal is routed, it shall be processed in the manner of analog signal. The shorter the routed, the better. and the adjacent reference layer shall be kept intact.		

1.22 Design Requirements on the LCD/BT video output circuit

Number	Items	Customer Confirmation (YES/NO)	Notes
1	T41 only supports Smart LCD, and the interface level only supports 3.3V.		
2	Smart LCD supports 8bit RGB888, RGB565 data access mode, and supports type A and type B interfaces.		
3	BT supports BT1120 and BT656 output, detailed data sequence connection method refer to the hardware schematic design.		
4	The above three video output interfaces are multiplexed on the same set of pins, so only one video output interface can be selected at the same time.		
5	PCLK signal needs 33R resistor in series at the source endpoint to adjust the impedance to obtain better signal quality.		

1.23 Design Requirements on the EFUSE power supply

Number	Items	Customer Confirmation (YES/NO)	Notes
1	EFUSE_AVDD is the OTP burning power supply with a typical voltage of 1.8V. The content chip in OTP has been burned and written when leaving the factory. In the product stage, it needs to connect to GND through 33R resistor, and the content of OTP is in read-only state.		

1.24 Design Requirements on Power Supplies and GND

Number	Items	Customer Confirmation (YES/NO)	Notes
1	VDD: T41 Core power supply, power supply chip selection requires that the power supply capacity is not less than 1A DCDC design.		
2	VDDMEM, DDRVDD: T41 DDR power supply, power supply chip selection requires that the power supply capacity is not less than 1A DCDC design.		
3	Magnetic beads are used to isolate PLL_VDD from the VDD core power supply, and magnetic beads are used to isolate PLL_AVDD from the 1.8V power supply.		
4	Magnetic beads are used to isolate between Codec_AVDD and 1.8V power supply, between CSI_VCC18 and 1.8V power supply, and between CSI_VCC09 and 0.9V power supply.		
5	VDD, VDDMEM, DDRVDD need to wire the power plane, there should be a sufficient number of power through holes, the power plane should ensure		

	sufficient width (greater than 40mil), no power bottleneck on the power plane.		
6	The adjacent layers of the Master chip are suggested to allocate GND layers. The VSS pins should make as many GND vias directly to the GND layer as possible, and ensure that there are enough GND planes in the GND vias of each layer to increase the thermal path of the Master chip .		